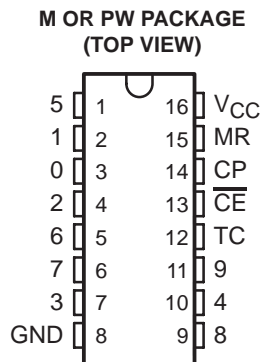


# CD74HC4017-Q1

## HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER WITH 10 DECODED OUTPUTS

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- Qualified for Automotive Applications
- Fully Static Operation
- Buffered Inputs
- Common Reset
- Positive Edge Clocking
- Typical  $f_{MAX} = 60$  MHz at  $V_{CC} = 5$  V,  $C_L = 15$  pF,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- $V_{CC}$  Voltage = 2 V to 6 V
- High Noise Immunity  $N_{IL}$  or  $N_{IH} = 30\%$  of  $V_{CC}$ ,  $V_{CC} = 5$  V



### description/ordering information

The CD74HC4017 is a high-speed silicon-gate CMOS 5-stage Johnson counter with ten decoded outputs. Each of the decoded outputs normally is low and sequentially goes high on the low-to-high transition clock period of the ten-clock-period cycle. The carry (TC) output transitions low to high after output 9 goes from high to low, and can be used in conjunction with the clock enable ( $\overline{CE}$ ) input to cascade several stages.  $\overline{CE}$  disables counting when in the high state. A master reset (MR) input also is provided that, when taken high, sets all the decoded outputs, except output 0, to low.

The device can drive up to ten low-power Schottky equivalent loads.

### ORDERING INFORMATION†

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – M	Tape and reel		
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC4017QM96Q1	HC4017Q
	TSSOP – PW	Tape and reel	CD74HC4017QPWRQ1	HC4017Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

### FUNCTION TABLE

INPUTS			OUTPUT STATE†
CP	$\overline{CE}$	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H, 1–9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

NOTE: H = high voltage level, L = low voltage level, X = don't care, ↑ = transition from low to high level, ↓ = transition from high to low level

† If  $n < 5$ , TC = H, otherwise TC = L



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**TEXAS  
INSTRUMENTS**

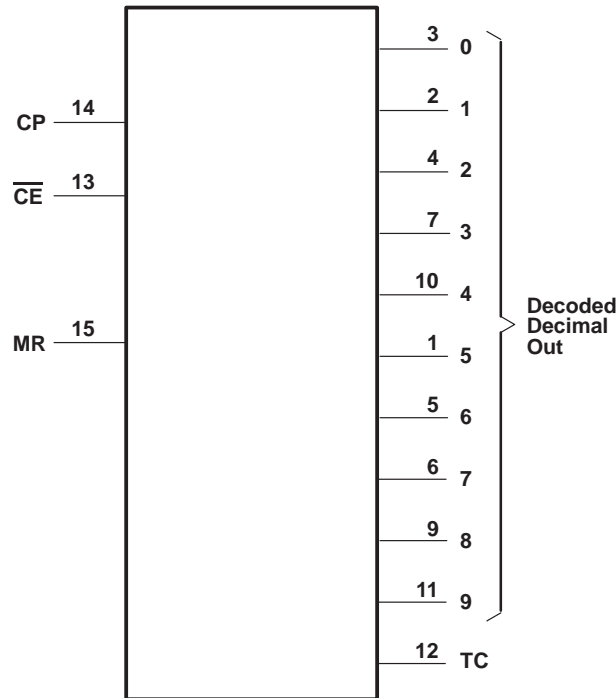
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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 20$ mA
Source or sink current per output pin, $I_O$ ( $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): M package	73°C/W
PW package	108°C/W
Maximum junction temperature, $T_J$	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10 s max	300°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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## HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER WITH 10 DECODED OUTPUTS

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### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	2	6	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V	
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V	
		V <sub>CC</sub> = 4.5 V	1.35		
		V <sub>CC</sub> = 6 V	1.8		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V	
t <sub>t</sub>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6 V	0	400	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C	

NOTES: 3. All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	I <sub>O</sub> (mA)	V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
				MIN	MAX			
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	-0.02	2 V	1.9	1.9	V	
			-0.02	4.5 V	4.4	4.4		
			-0.02	6 V	5.9	5.9		
		TTL loads	-4	4.5 V	3.98	3.7		
			-5.2	6 V	5.48	5.2		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	0.02	2 V	0.1	0.1	V	
			0.02	4.5 V	0.1	0.1		
			0.02	6 V	0.1	0.1		
		TTL loads	4	4.5 V	0.26	0.4		
			5.2	6 V	0.26	0.4		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		6 V	±0.1	±1	μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0	6 V	8	160	μA		
C <sub>IN</sub>	C <sub>L</sub> = 50 pF			10	10	pF		



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
				MIN	MAX			
f <sub>max</sub> Maximum clock frequency			2 V	6		4		MHz
			4.5 V	30		20		
			6 V	35		23		
t <sub>w</sub>	Pulse duration	CP	2 V	80		120		ns
			4.5 V	16		24		
			6 V	14		20		
	MR	2 V	80		120			
		4.5 V	16		24			
		6 V	14		20			
t <sub>su</sub>	Setup time	$\overline{\text{CE}}$ to CP	2 V	75		110		ns
			4.5 V	15		22		
			6 V	13		19		
	MR inactive	2 V	5		5			
		4.5 V	5		5			
		6 V	5		5			
t <sub>h</sub>	Hold time, $\overline{\text{CE}}$ to CP		2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		



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## HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER WITH 10 DECODED OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
					MIN	TYP	MAX				
t <sub>pd</sub>	CP	Decade out	C <sub>L</sub> = 50 pF	2 V		230		345	ns		
				4.5 V		46	69				
				6 V		39	59				
			C <sub>L</sub> = 15 pF	5 V		19					
				TC	C <sub>L</sub> = 50 pF	2 V		230			345
						4.5 V		46		69	
		6 V				39	59				
		C <sub>L</sub> = 15 pF	5 V			19					
			Decade out		C <sub>L</sub> = 50 pF	2 V		250			375
						4.5 V		50		75	
		6 V				43	64				
		C <sub>L</sub> = 15 pF		5 V		21					
	TC			C <sub>L</sub> = 50 pF	2 V		250			375	
					4.5 V		50	75			
		6 V			43	64					
		C <sub>L</sub> = 15 pF	5 V		21						
			MR	Decade out	C <sub>L</sub> = 50 pF	2 V		230			345
						4.5 V		46		69	
	6 V					39	59				
	C <sub>L</sub> = 15 pF	5 V				19					
		TC			C <sub>L</sub> = 50 pF	2 V		230			345
						4.5 V		46		69	
	6 V					39	59				
	C <sub>L</sub> = 15 pF			5 V		19					
TC, Decade out				C <sub>L</sub> = 50 pF	2 V		75		110		
					4.5 V		15	22			
	6 V				13	19					
f <sub>max</sub>	CP			C <sub>L</sub> = 15 pF	5 V		60		MHz		

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, input t<sub>r</sub>, t<sub>f</sub> = 6 ns, C<sub>L</sub> = 15 pF

PARAMETER	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance (see Note 4)	39	pF

NOTE 4: C<sub>pd</sub> is used to determine the dynamic power consumption per package.

$$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

f<sub>i</sub> = input frequency

f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

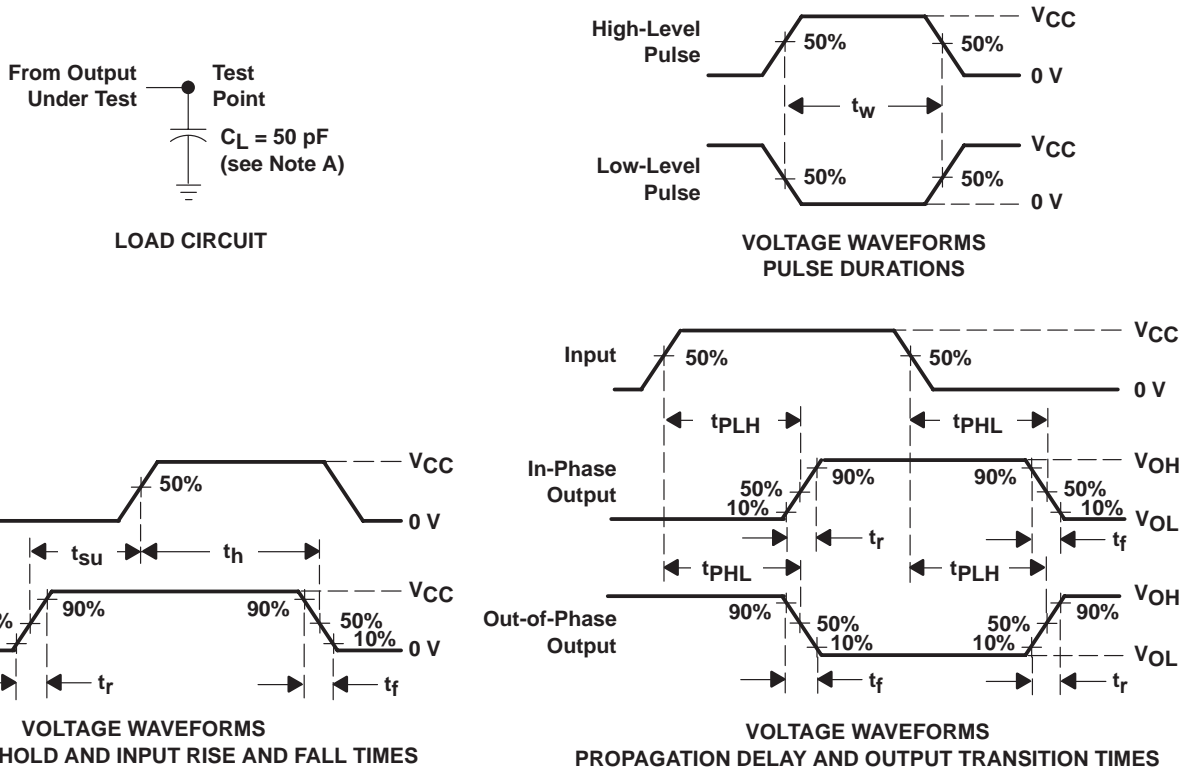
V<sub>CC</sub> = supply voltage



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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

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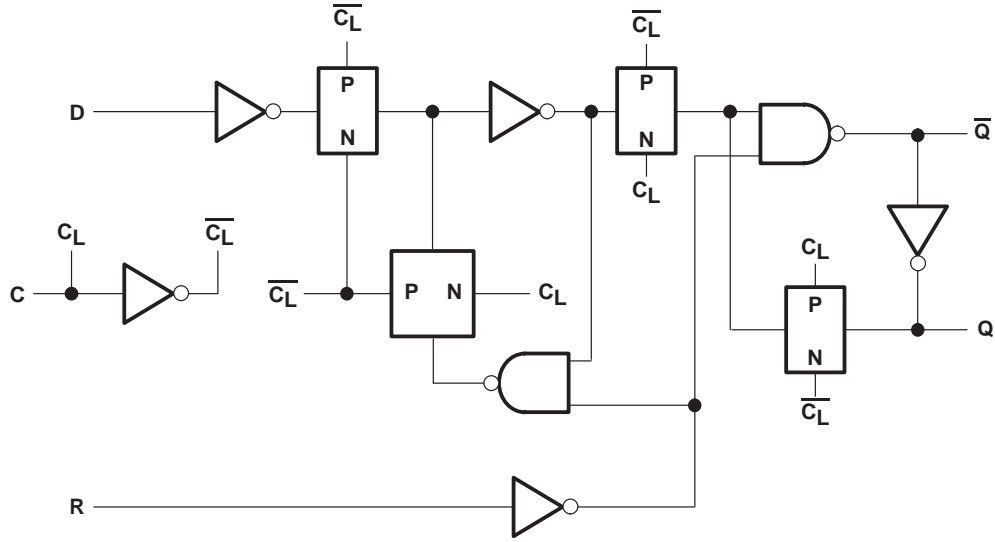


Figure 2. Flip-Flop Detail

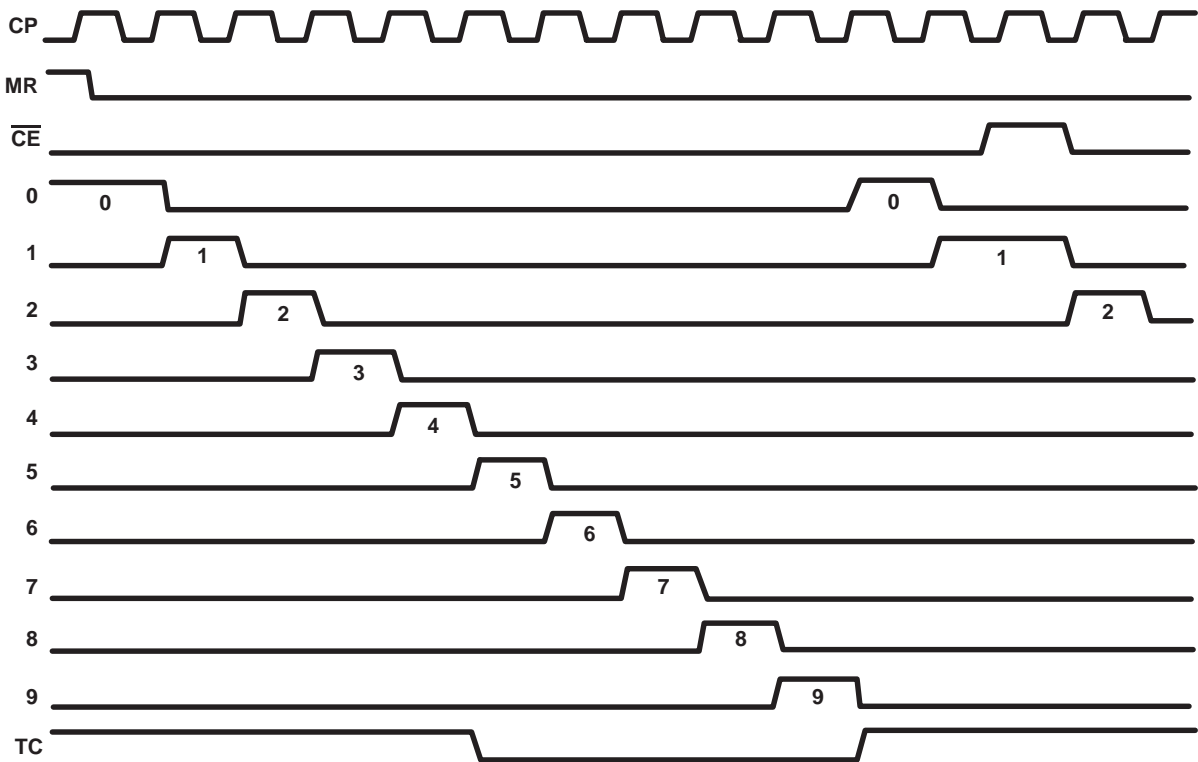


Figure 3. Timing Diagram

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74HC4017QM96G4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4017QM96Q1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74HC4017QPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4017QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Enhanced Product: [CD74HC4017-EP](#)
- Military: [CD54HC4017](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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